Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-18 (Canceled)

Claim 19 (Previously Presented): A capacitor comprising:

a first metal plate formed above a semiconductor substrate;

a second metal plate formed above the first metal plate, the second metal plate having an opening in a central portion thereof;

a third metal plate formed above the second metal plate;

an insulating material between the first, second and third metal plates and on the semiconductor substrate; and

a conductive member, formed through the insulating material and the opening of the second metal plate, that electrically connects the first and third metal plates.

Claim 20 (Currently Amended): The capacitor of claim 19, further comprising:

a bottom conductive pattern formed [[on]] over the semiconductor substrate; and

a second conductive member, formed through the insulating material, that electrically connects the first metal plate and the bottom conductive pattern.

Claim 21 (Previously Presented): The capacitor of claim 20, wherein the bottom conductive pattern comprises a polysilicon interconnection pattern formed on an oxide layer over the semiconductor substrate.

Claim 22 (Previously Presented): The capacitor of claim 20, wherein the bottom conductive pattern comprises a metal interconnection pattern formed on an oxide layer over the semiconductor substrate.

Claim 23 (Previously Presented): The capacitor of claim 20, wherein the bottom conductive pattern comprises a diffusion pattern formed in the semiconductor substrate.

Claim 24 (Previously Presented): The capacitor of claim 19, wherein each of the first and third metal plates have larger area than an area of the second metal plate.

Claim 25 (Previously Presented): The capacitor of claim 19, wherein the second metal plate is divided into plate sections that are electrically isolated from each other.

Claim 26 (Previously Presented): The capacitor of claim 19, used as a unit capacitor within a capacitor array of plural unit capacitors.

Claim 27 (Previously Presented): The capacitor of claim 26, wherein the second metal plate has conductive branch members extending therefrom that connect the second metal plate to second metal plates of the plural unit capacitors.

Claim 28 (Previously Presented): The capacitor of claim 27, wherein the first, second and third metal plates are rectangular shaped, the second metal plate having respective conductive branch members extending from each side thereof.

Claim 29 (Previously Presented): The capacitor of claim 27, wherein the second metal plate is divided into plate sections, the plate sections being electrically isolated from each other.

Claim 30 (Previously Presented): A capacitor array including a plurality of interconnected unit capacitors, each of the unit capacitors comprising:

a first metal plate formed above a semiconductor substrate;

a second metal plate formed above the first metal plate, the second metal plate having an opening in a central portion thereof;

a third metal plate formed above the second metal plate;

an insulating material between the first, second and third metal plates and on the semiconductor substrate; and

a conductive member, formed through the insulating material and the opening of

the second metal plate, that electrically connects the first and third metal plates.

Claim 31 (Currently Amended): The capacitor array of claim 30, further comprising:

a plurality of bottom conductive patterns formed [[on]] over the semiconductor substrate; and

a plurality of second conductive members, formed through the insulating material, that electrically connect the first metal plates and the bottom conductive patterns.

Claim 32 (Previously Presented): The capacitor array of claim 31, wherein the bottom conductive patterns comprise polysilicon interconnection patterns formed on oxide layers over the semiconductor substrate.

Claim 33 (Previously Presented): The capacitor array of claim 31, wherein the bottom conductive patterns comprise metal interconnection patterns formed on oxide layers over the semiconductor substrate.

Claim 34 (Previously Presented): The capacitor array of claim 31, wherein the bottom conductive patterns comprise diffusion patterns formed in the semiconductor substrate.

Claim 35 (Previously Presented): The capacitor array of claim 30, wherein each of the

first and third metal plates have larger area than an area of the second metal plates.

Claim 36 (Previously Presented): The capacitor array of claim 30, wherein the second metal plates have conductive branch members extending therefrom that connect the second metal plates of the unit capacitors together.

Claim 37 (Previously Presented): The capacitor array of claim 36, wherein the first, second and third metal plates are rectangular shaped, the second metal plates having respective conductive branch members extending from each side thereof.

Claim 38 (Previously Presented): The capacitor array of claim 30, comprising unit capacitors connected at a periphery of the capacitor array as dummy unit capacitors,

the second metal plates of the dummy unit capacitors being divided into dummy plate sections, so that dummy plate sections of a respective dummy unit capacitor are electrically isolated from other dummy plate sections of the respective dummy unit capacitor.

Claim 39 (Previously Presented): The capacitor array of claim 38, wherein only the dummy plate sections that are directly adjacent and facing the unit capacitors are electrically connected to the second metal plates of corresponding adjacent unit capacitors.

Claim 40 (Previously Presented): The capacitor array of claim 39, wherein the dummy plate sections that are not directly adjacent and facing the unit capacitors are grounded or electrically floating.

Claim 41 (Previously Presented): The capacitor array of claim 39, wherein the second metal plates of the unit capacitors are rectangular shaped and include respective conductive branch members extending from each side thereof, the second metal plates of the corresponding adjacent unit capacitors being electrically connected to the dummy plate sections of the dummy unit capacitors via the conductive branch members.